PVP 19

Code: 19EC3602

III B.Tech - II Semester – Regular Examinations – JUNE 2022

INTRODUCTION TO VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 5 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each question carries 12 marks.
4. All parts of Question paper must be answered in one place.

PART – A

1. a) Discuss the difference between blocking and non-blocking assignments with an example.
   b) What is an advantage of CPLD over an FPGA?
   c) Draw the transistor circuit symbols for nMOS enhancement, nMOS depletion.
   d) Draw the stick diagram of CMOS inverter.
   e) What are the differences between constant voltage scaling and constant field scaling?

PART – B
UNIT – I

2. a) Write a Verilog gate-level model of a circuit that will produce two outputs, *d* and *b*, equal to the difference and borrow produced by subtracting two binary input bits *a* and *b.* 6 M
   b) Design 4-bit counter using Verilog-HDL code. 6 M

OR

3. a) Write a Verilog HDL gate-level program to simulate the 4:1 multiplexer. 6 M

b) Write the stimulus block/test bench to verify the above 4:1 multiplexer. 6 M

UNIT – II

4. a) Explain the CPLD general architecture. 6 M

b) Discuss the function blocks architecture. 6 M

OR

5. a) Explain the FPGA general architecture. 6 M

b) Draw the internal structure of Configurable Logic Block. 6 M

UNIT-III

6. a) With neat sketches, explain the fabrication steps involved in NMOS fabrication process. 6 M

b) Compare the performance of CMOS and BiCMOS technologies. 6 M

OR

7. Explain the CMOS fabrication process in detail. 12 M

UNIT – IV

8. a) Derive MOS transistor conductance g_m and output conductance g_{ds}. 6 M

b) In the inverter circuit: what is meant by Zp.u. and Zp.d.? Derive the required ratio between Zp.u. and Zp.d. if an nMOS inverter is to be driven from another nMOS inverter. 6 M

OR

9. a) Draw the Layout diagram of CMOS inverter at 2μm micron based design rules. 6 M

b) Specify the minimum design rules for all layers in lamda (λ) based rules. 6 M

UNIT – V

10. a) Explain how device dimensions are scaled in constant field scaling. 6 M

b) Explain the short channel effects due to scaling. 6 M

OR

11. a) Design a 3 bit even parity generator. 6 M

b) Implement the Ex-OR gate using switch level logic. 6 M